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A NOVEL RAM CELL DESIGN IN QUANTUM-DOT CELLULAR AUTOMATA

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ABSTRACT: *In the era of nano-computing, there has been widespread work to illustrate the Quantum dot-cellular automata (QCA) based design of various digital circuits and their functionality. Since the emergence of this technology in 1993 QCA has achieved their fame in designing low-power nano-devices for logic computation and digital systems. Subsequently, one of the substantial components of any digital system is memory. Therefore, designing a well-optimized and high speed QCA random access memory (RAM) is of utmost importance. In this paper a novel design of the RAM cell in QCA is introduced. The design and the simulation of the said block is done QCA Designer tool (v 2.0.3) environment.*

KEYWORDS: *Quantum dot cellular automata, Digital Memory, RAM, FNZ universal gate.*

1. INTRODUCTION

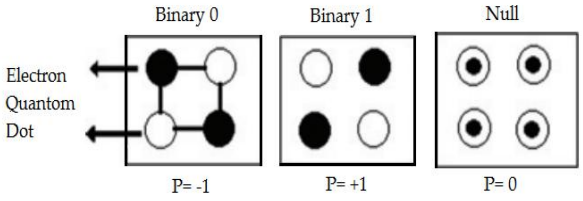
The raise of the interest in devising the computing circuits at nano-scale has lead into the gain of popularity of QCA owing to the inherent advantage of QCA over conventional integrated circuit technologies at nano-scale level. Despite the ambiguities, whether QCA will be able to replace the well-established technologies of today, still a lot of investigation is going on in the researchers and scientists which have revealed that QCA has many powerful features some of which are not there in CMOS [1], [2]. The main issue with QCA is its physical implementation but a lot of work is taking place in this regard. Of many features of the QCA like the simple design, one of the attractive feature of QCA is that there is no fixed connection strategy which results in the possibility of applying optimization algorithms to minimize the number of cells in the design.

Up to now, lot of the study has been performed on QCA and its circuits design and structures [1–15], and Memory cells forms one of the vital areas in designing QCA circuits. In [7–15] various QCA flip flops and memory cells have been introduced. The main aim of this paper is to present efficient designs of the Random Access Memory units in QCA. The remainder of this paper is organized as follows: a brief overview on QCA is presented in Section 2 along with the brief introduction on FNZ gate. The proposed RAM structures are proposed in Section 3. Finally, section 4 compares of the conclusion.

2. QCA OVERVIEW

QCA consists of an array of cells. Each cell is composed of several quantum dots (typically four), each of which is a nanoparticle or a crystal (made of semiconducting materials such as silicon, cadmium selenide etc.) and every quantum dots is covered by an insulating material [16-18]. Each cell is connected through a metallic tunneling wire by way of which the electron can tunnel from one dot to another dot, as shown in Figure

1. For cell polarization, first of all two free extra electrons are placed within a QCA cell. As the electrons have a repulsive force on each other, they position themselves at opposite corners within the QCA cell. The two possible positions of the electrons mean there are two different QCA cell structures, called the QCA cell's polarization denoted by Pas shown in Figures 1(a) and 1(b). Depending on the value of P, the QCA cell can hold logic values 1 and 0. If P = +1, then the logic value 1 is stored within a QCA cell, and if P = −1, then the logic value 0 is stored. P = 0 indicates an unpolarized cell – that is, it contains no information, [16, 17, 19-21] as shown in Figure 1(c).

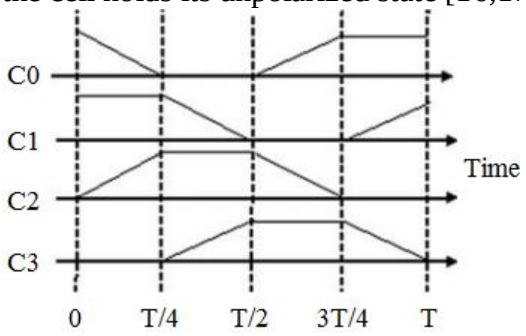


(a) (b) (c)

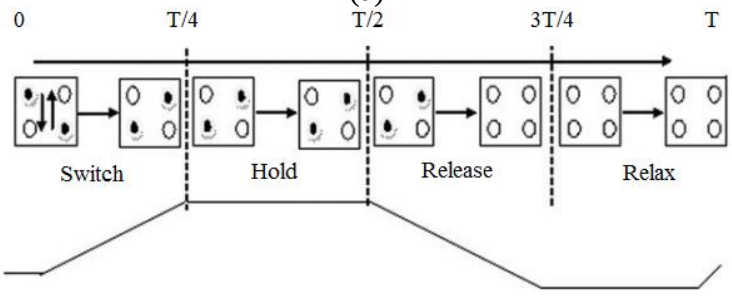
Figure1. Different QCA cell polarizations

2.1 QCA Clocking

In QCA, adiabatic switching happens, [16-18] and the switching is done in four clocking zones lagging by p/2, [19-21] as shown in Figure 2. This is helpful in designing a nano-circuit in a different way than traditional CMOS circuits. In the switch phase, the QCA cell starts to gain its polarization as the barrier between the dots is gradually raised, and the electrons start tunneling between the dots. In the hold phase, the cell polarization gained from the previous phase remains the same–that is, fixed polarization–as the barrier between the dots remains high, and the tunneling of electrons is prohibited. In the release phase, the QCA cell sets out to an unpolarized state from the polarization state as the barrier between the dots is in a lowered condition, and the electrons now have the ability to tunnel between the dots. In the relax phase, the barrier between the dots remains at a lowered condition, and the cell holds its unpolarized state [16,17].



(a)

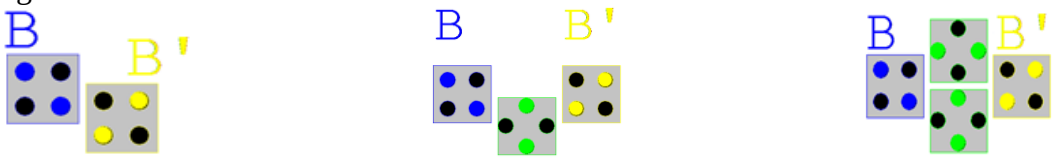


(b)

Figure2. QCA clocking: (a) Four-phase (b) working procedure during one clock phase

2.2 Qca Inverter

Till date various QCA based inverter designs have been introduced in the open literature. Few of the designs are given in Figure 3. The input signal 'B' is provided from left side, and the inverted output 'B'' emerges at the right side.



(a) (b) (c)

Figure3. QCA implementation of Inverters

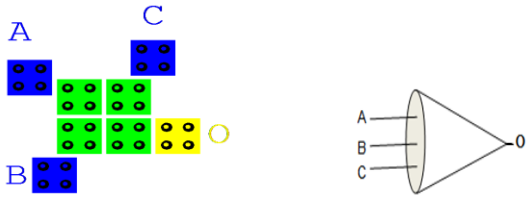
2.3 FNZ Gate:

Most of the circuit implementations in QCA are achieved using the following QCA universal gates.

- Majority Voter (MV)
- AND-OR-Invert (AOI)
- NAND-NOR-INVERT (NNI)

The first technique has been employed in majority of the published research work and the next two techniques have been derived from the first technique itself. Recently a novel universal gate was introduced by Farooq et al. [22] named as FNZ gate. The paper besides introducing the universal gate for QCA also claimed that the gate is highly effective regarding area, density, power, latency and complexity space and speed consideration. It provides a significant reduction in hardware cost and switching delay with respect to the other existing techniques. The QCA design and the symbol of FNZ gate are given in Figure 4 (a) and 4 (b) respectively. The logical expression for FNZ gate is given in (1) as

$$F = A'B' + (A \oplus B)C \quad (1)$$



(a) (b)

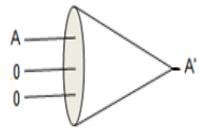
Figure 4: FNZ Gate (a) QCA Design, and (b) Symbol

In this paper, design of the RAM cell using FNZ gate is achieved and for this we need logic operators like NOT, NAND and NOR. The implementation of these operations using the FNZ gate is given in Table 2. The truth table of FNZ gate is given in table 1, as under

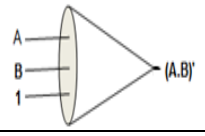
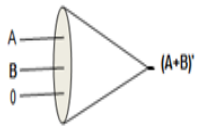
Table 1:

Truth Table			
A	**B**	**C**	**O**
0	0	0	**1**

Table 2:

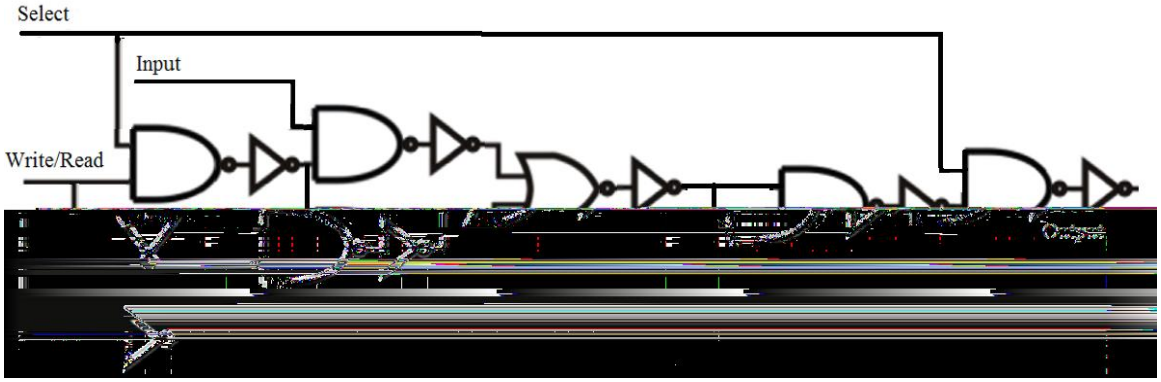
NOT	A'	FNZ(A,0,0)	

0	0	1	**1**
0	1	0	**0**
0	1	1	**1**
1	0	0	**0**
1	0	1	**1**
1	1	0	**0**
1	1	1	**0**

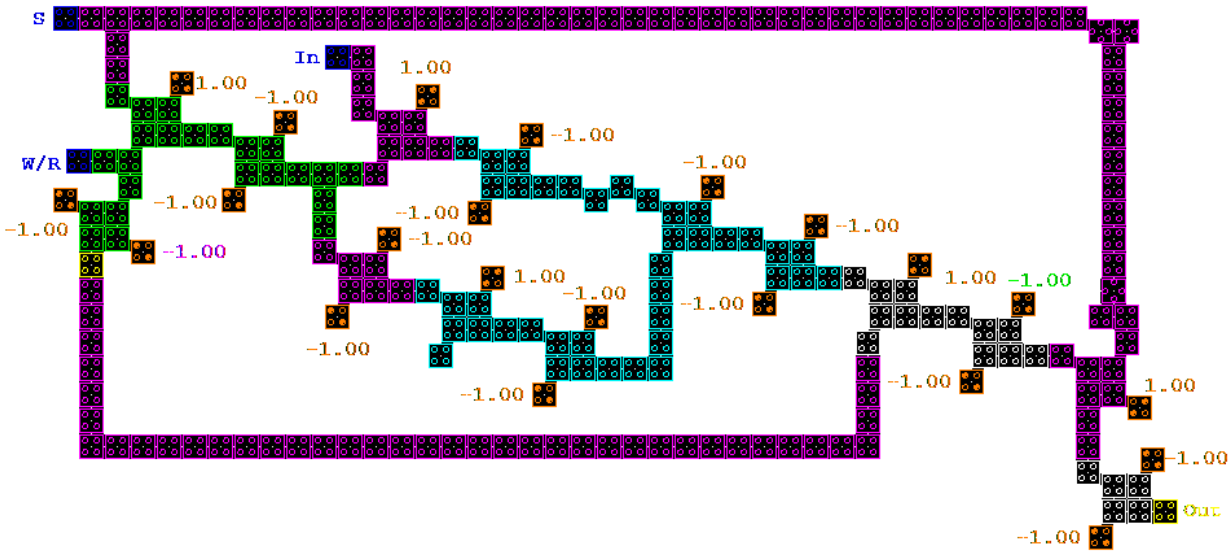
NAND	$(A.B)'$	FNZ(A,B,1)	
NOR	$(A+B)'$	FNZ (A,B,0)	

3. PROPOSED QCA RAM CELLS

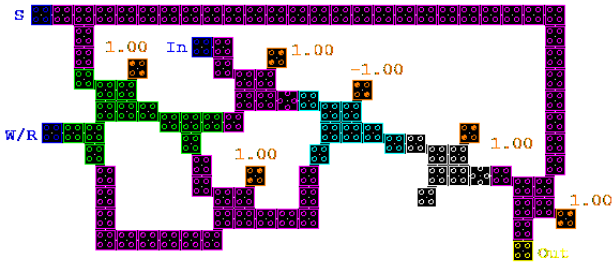
RAM cell design is one of the most attractive fields of study in QCA. The schematic for the proposed RAM cell structure and QCA implementation of that are indicated in Figure 5 (a) and 5 (b) respectively. The design is composed of NAND, NOR and Inverter Logics and to achieve the QCA design we have simply utilized NAND, NOR and Inverter circuits of Table 2. Figure 5 (c) represents the QCA implementation of the same structure with the reduced cell counts. In this design we have made use of the inverter cells of Figure 3. Similarly, the schematic for the proposed RAM cell structure with set and reset ability and QCA implementation of that are indicated in Figure 6 (a) and 6 (b) respectively while as Figure 6 (c) represents the QCA implementation of the RAM cell structure with set and reset ability with the reduced cell counts.



(a)

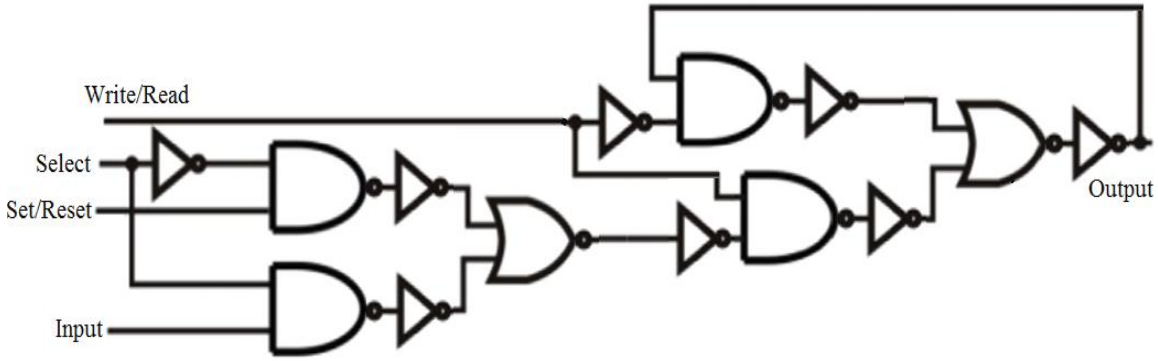


(b)

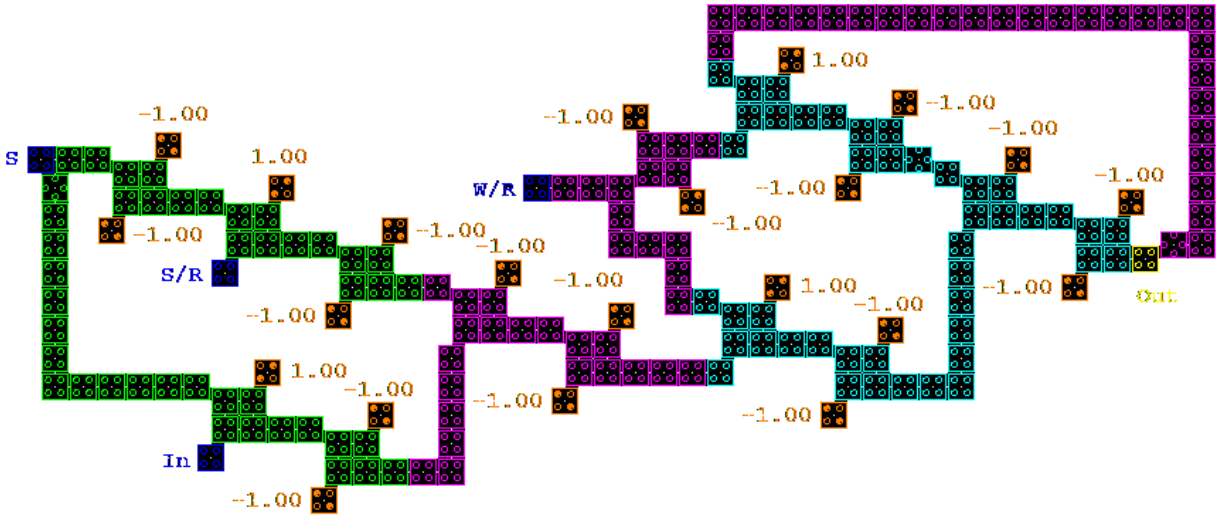


(c)

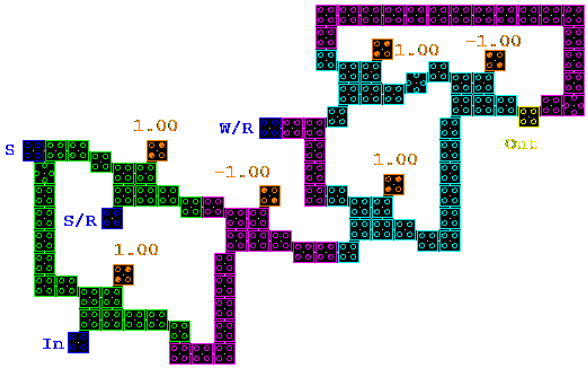
Figure 3: The RAM cell structure (a) schematic diagram, (b) FNZ based QCA Implementation, and (c) FNZ based QCA Implementation with reduced cell count.



(a)



(b)



(c)

Figure 4: The RAM cell structure with set and reset ability (a) schematic diagram, (b) FNZ based QCA Implementation, and (c) FNZ based QCA Implementation with reduced cell count.

CONCLUSION

In this paper, a novel FNZ base RAM memory cells with and without set/reset ability were introduced. The proposed designs have efficient structures in terms of area, delay and complexity (cell count). The design can further be extended for their use in digital circuits.

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